CLAIMS:

What is claimed is:

1. A data processing system for qualifying events when an interrupt occurs, comprising:

a performance monitoring unit;

one or more hardware counters located within the performance monitoring unit;

wherein the one or more hardware counters count the occurrence of events during an interrupt of a selected type.

2. The system of claim 1, wherein the one or more hardware counters count the occurrence of events during a state of the interrupt of the selected type.

3. The system of claim 2, wherein states of the interrupt include accepting the signal, invoking an interrupt handler routine of the interrupt, completion of the interrupt handler routine, and interrupt return.

4. The system of claim 1, wherein multiple types of events are counted during the interrupt.

5. The system of claim 1, wherein the one or more hardware counters count the occurrence of events according to the type of interrupt during which they occur.

6. The system of claim 1, wherein the events include clock cycles and cache misses.

7. The system of claim 1, wherein a second interrupt interrupts a first interrupt, and wherein the hardware counters count events separately that occur during the first and second interrupts.

8. A method of executing instructions on an information processing system, comprising the steps of:

receiving a signal at a microprocessor of the system for invoking an interrupt, wherein the interrupt includes a plurality of states; and

counting at least one event for a selected state of the plurality of states for the interrupt.

9. The method of claim 8, wherein the step of counting includes at least one event for each of the plurality of states of the interrupt

10. The method of claim 8, wherein the plurality of states include accepting the signal, invoking an interrupt handler routine of the interrupt, completion of the interrupt handler routine, and interrupt return.

11. The method of claim 8, wherein the at least one event includes clock cycles and cache misses.

12. The method of claim 8, wherein the step of counting includes counting multiple types of events for the same state of the interrupt.

13. The method of claim 8, wherein the step of counting is performed by one or more hardware counters.

14. The method of claim 8, wherein the events are counted according to the type of interrupt during which they occur.

15. The method of claim 8, wherein a first interrupt is interrupted by a second interrupt, and wherein hardware counters count events separately that occur during the first and second interrupts.

16. A computer program product in a computer readable medium for processing instructions, the computer program product comprising:

first instructions for receiving a signal at a microprocessor of the system for invoking an interrupt, wherein the interrupt includes a plurality of states; and

second instructions for counting at least one event for a selected state of the plurality of states for the interrupt.

17. The computer program product of claim 15, wherein the plurality of states include accepting the signal, invoking an interrupt handler routine of the interrupt,

completion of the interrupt handler routine, and interrupt return.

18. The computer program product of claim 15, wherein the at least one event includes clock cycles and cache misses.

19. The computer program product of claim 15, wherein the second instructions for counting count multiple types of events for the same state of the interrupt.

20. The computer program product of claim 15, wherein the step of counting is performed by one or more hardware counters.

21. The computer program product of claim 15, wherein the events are counted according to the type of interrupt during which they occur.

22. The method of claim 15, wherein a first interrupt is interrupted by a second interrupt, and wherein hardware counters count events separately that occur during the first and second interrupts.